

ASIC Core Library

Product Letter

RISC CPU

ARM7TDMI 32-bit Core

Description

The ARM7TDMI is an ARM7 32-bit RISC processor core with the Thumb extension, Embedded ICE for 'in ASIC' debugging and a DSP enhanced multiplier. Thumb offers 32-bit RISC performance at 16-bit system cost through a "compression" of the original ARM7 instruction set that results in excellent code density and thus saves memory space. On execution, 16-bit Thumb instructions are "decompressed" transparently on the fly into full 32-bit ARM7 instructions. Designers can select between ARM and Thumb modes during execution for optimum price/performance balancing.

The performance of the ARM7TDMI microprocessor core depends whether the code uses Thumb or ARM instruction set. Furthermore it depends on the used memory width. In a 32-bit wide memory system with no wait states, Dhystone 2.1 gives the following results depending of the clock frequency.

Performance

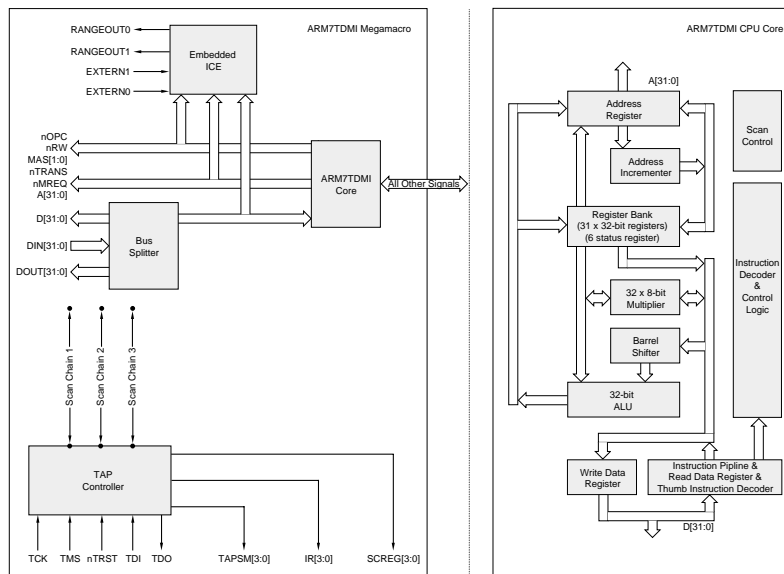
Instruction type	P _{DHRY} (MCLK)	@ 33 MHz
ARM	0.9 MIPS/MHz	29.7 MIPS
Thumb	0.74 MIPS/MHz	24.4 MIPS

The maximum clock frequency depends on the target technology and is in the range of 30/40/50 MHz for 0.5 μ /0.35 μ /0.25 μ CMOS technology under worst case operating conditions.

Features

- 32-bit operand size and internal bus width
- 8/16/32-bit Memory I/F
- 32-bit (ARM) / 16-bit (Thumb) Instruction width
- 16 User Registers
- 32-bit x 8-bit Multiplier
- 4 Gbyte Addressing Space
- 3-stage Instruction Pipeline
- Barrel Shifter and Rotate Instruction for DSP algorithm support

Block Diagram



System @ IC
Solutions on a Chip

NEC

NEC Offices

NEC Electronics (Europe) GmbH, Oberrather Str. 4, D-40472 Düsseldorf,
Tel. (02 11) 65 03 01, Fax (02 11) 65 03-327

NEC Electronics (Germany) GmbH, Kanzlerstr. 2, D-40472 Düsseldorf,
Tel. (02 11) 65 03 02, Fax (02 11) 65 03-490
- Podbielskistr. 164, D-30177 Hannover, Tel. (05 11) 33 40 2-0, Fax (05 11) 33 40 2-34
- Arabellastr. 17, D-81925 München, Tel. (089) 92 10 03-0, Fax (089) 91 31 82
- Industriestr. 3, D-70565 Stuttgart, Tel. (07 11) 9 90 10-0, Fax (07 11) 9 90 10-19

NEC Electronics (BNL) - Boschdijk 187a, NL-5612 HB Eindhoven,
Tel. (0 40) 2 44 58 45, Fax (0 40) 244 45 80

NEC Electronics (Scandinavia) - Täby Centrum, Entrance S (7th floor),
S-18322 Täby, Tel. (8) 638 08 20, Fax (8) 638 03 88

NEC Electronics (France) S.A., 9, rue Paul Dautier, B.P. 187,
F-78142 Velizy-Villacoublay Cédex, Tél. (01) 30 67 58 00, Fax (01) 30 67 58 99

NEC Electronics (France) S.A., Representacion en Espana,
Juan Esplandiu 15, E-28007 Madrid, Tel. (01) 5 04 27 87, Fax (01) 5 04 28 60

NEC Electronics Italiana S.R.L., Via Fabio Filzi, 25A, I-20124 Milano,
Tel. (02)66 75 41, Fax (02) 66 75 42 99
- Rome Office, Via Monte Cervialto, 131, I-00139 Roma,
Tel. (06) 8 86 22 91/2, Fax (06) 8 86 22 39

NEC Electronics (UK) Ltd., Cygnus House, Sunrise Park Way, Milton Keynes,
GB-MK14 6NP, Tel. (01 908) 69 11 33, Fax (01 908) 67 02 90
- Scotland Office, Block 3, Carfin Industrial Estate Motherwell GB-ML1 4UL,
Tel. (01 698) 73 22 21, Fax (01 698) 83 38 68

Internet: <http://www.nec.de>

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