

ASIC Core Library

Product Letter

RISC CPU

ARM710T 32-bit Core with Cache

Description

The ARM710T is a general-purpose 32-bit microprocessor with 8 KB cache, enlarged write buffer and Memory Management Unit (MMU) combined in a single chip. The CPU within the ARM710T is the ARM7TDMI. The ARM710T is software compatible with the ARM processor family. Clock frequencies are almost identical with the ARM7TDMI core.

The on-chip mixed data and instruction cache, together with the write buffer, substantially raise the average execution speed and reduce the average amount of memory bandwidth required by the processor. This allows the external memory to support additional processors or Direct Memory Access (DMA) channels with minimal performance loss. The MMU supports a conventional two-level page-table structure and a number of extensions which make it ideal for embedded control, UNIX and object oriented systems.

ARM710T is a fully static part and has been designed to minimise power requirements. This makes it ideal for portable applications where both these features are essential.

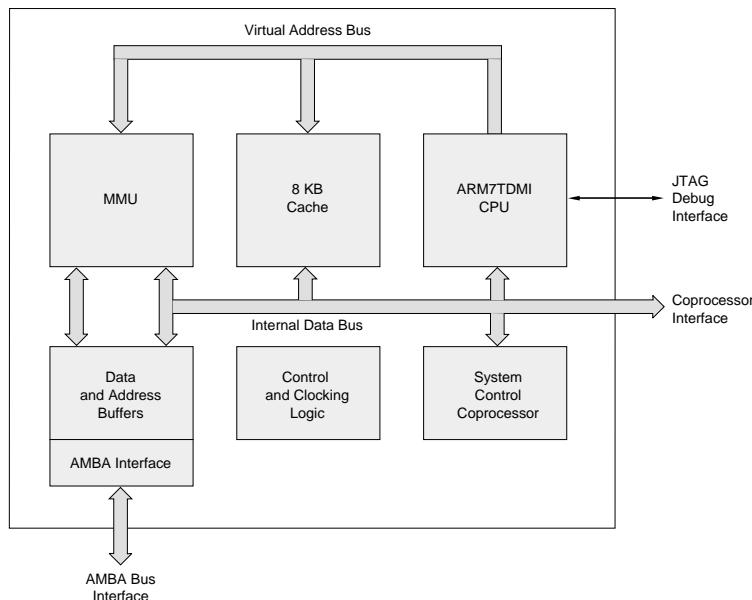
Cache

ARM710T contains an 8 KB mixed instruction and data cache (IDC). The IDC has 512 lines of 16 bytes (four words), arranged as a four-way set-associative cache, and uses the virtual addresses generated by the processor core. The IDC is always reloaded a line at a time (four words). It may be enabled or disabled via the ARM710T Control Register. The operation of the cache is further controlled by the cacheable (C) bit stored in the Memory Management Page Table. For this reason, the MMU must be enabled in order to use the IDC.

MMU

The MMU performs two primary functions a) it translates virtual addresses into physical addresses and b) it controls memory access permissions. The MMU hardware required to perform these functions consists of a translation look-aside buffer, access control logic and translation-table-walking logic. The MMU supports memory accesses based on sections or pages. Sections are 1MB blocks of memory. Small pages consist of 4 KB blocks of memory while large pages consist of 64 KB blocks of memory.

Block Diagram



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Solutions on a Chip

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