

System-on-Chip

Product Letter

SYSTEM-ON-CHIP LITE

Design Flow

Introduction

System-on-Chip Lite (SoCLite) is NEC's new approach for low- to mid-volume SOC projects. Due to the fact, that the customer is required to design the UDL (User Defined Logic) area of the SoCLite device a smooth and easy design flow becomes important. The target is to integrate the customer specific UDL design together with the pre-designed SoCLite ARM subsystem to create a single chip custom controller. As in traditional gate-array ASICs, the UDL area consists of a pre-diffused sea-of-gates array. Custom logic is implemented by adding three metallization layers. SoCLite is targeting customers with Gate Array design experience as well as customers having so far focused on FPGA design. Therefore basically two different design flows are supported.

Gate Array Design Flow

The GA design flow is aimed at customers who have ASIC design experience and NEC's OpenCAD™ design environment required for GA design. The SoCLite UDL design flow starts with the design input in form of VHDL. The design is simulated at the behavioural (Register Transfer Level) or mixed (behavioural/gate) level and then synthesised down to the gate level. The UDL part can be simulated together with the SoCLite ARM subsystem by using a model for the subsystem provided by NEC. Before doing the UDL synthesis customers should verify the design using the SoCLite development board. Customers using the GA design flow will provide NEC the netlist of their UDL area design.

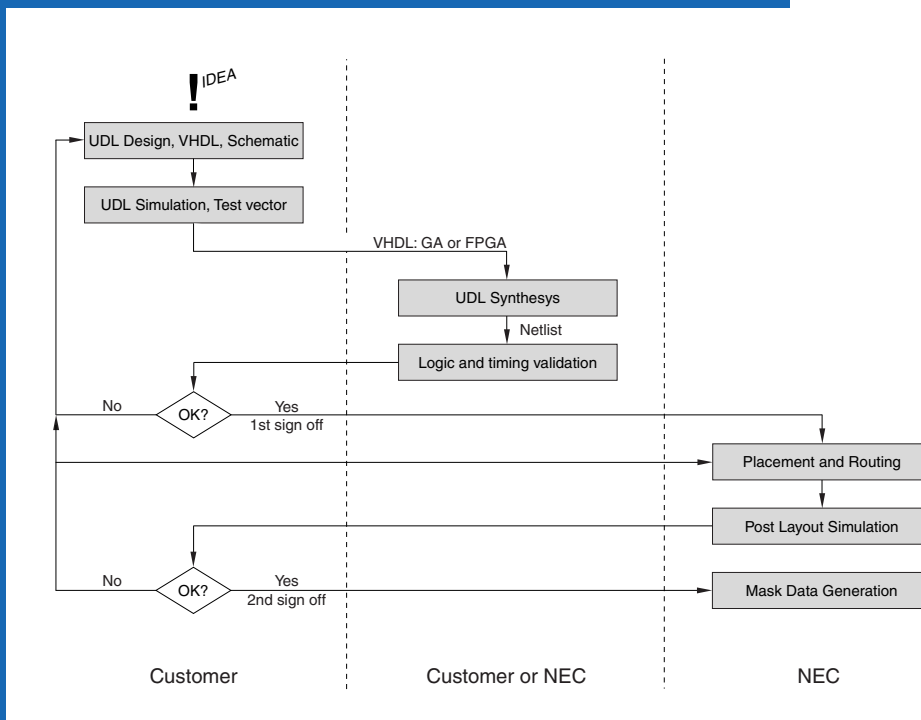
FPGA Design Flow

The FPGA design flow is aimed at customers who have not engaged in GA design so far, but have already designed FPGA's. The UDL area will be designed by the customer in VHDL using an FPGA from Xilinx or Altera. For the functional verification of their UDL design customer will use the SoCLite development board. The FPGA to GA conversion as well as the netlist synthesis will be done by one of the NEC design centers.



For further information on NEC products visit our European web-site at www.nec.de.

Block Diagram



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© Published by NEC Electronics (Europe) GmbH, Printed in Germany, January 2003
Document No. A15047EE1V2PL00

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