

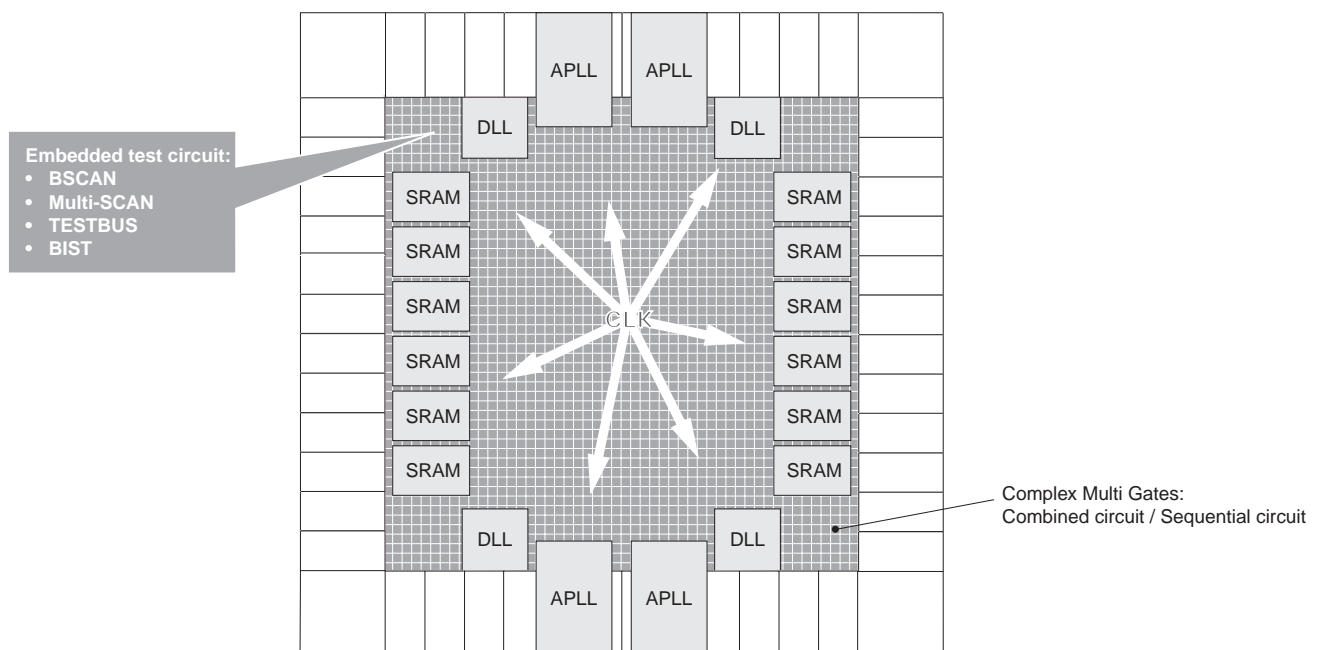
Description

NEC's Instant Silicon Solution Platform (ISSP) is an ASIC architecture, that offers high system performance – up to 150 MHz system frequency and up to 250 MHz for local areas – in 0.13 μm (drawn) gate length technology at low NRE. ISSP avoids the typical process-related hurdles of deep-sub-micron CB-IC ASIC designs by taking a new approach. Complex multi gates (CMGs) are prediffused on the base-array. For each base-array up to 7 metal layers are available: Two layers can be freely used for the customer logic, three layers are ready made for design for testability (DFT), signal integrity (SI) and power routing measures. Power and FCBGA lines can also be added on top. In addition ISSP designs are moved into volume production very quickly. In short, ISSP supports high-performance applications, featuring low NRE, and very short development and production times.

Features

- 0.13 μm (drawn) transistor gate length silicon gate CMOS process
- Up to 7 metal layers (layer 1-3 for signal integrity counter measures)
- 214 k to 1.7 M usable ASIC gates
- Up to 3.7 Mbit synchronous single- or dual-port RAM
- High-speed system frequency: up to 150 MHz system frequency and up to 250 MHz for local areas
- 1.5 V core voltage optimized architecture
- I/O voltage options: 1.5 V, 2.5 V, 3.3 V
- Flexible I/O structure supports LVTTTL, 2.5V CMOS, SSTL2/3, HSTL, LVDS, PECL, PCI-X
- Packaging: Tape BGAs (TBGA), advanced BGAs (ABGA) and Flip Chip BGAs
- Prediffused APLLs, DLLs
- Corrective measures against DSM effects, clock trees and DFT are embedded

Block Diagram



Product Outline

Base-array name	μPD65701	μPD65702	μPD65703	μPD65704/6	μPD65705/7
Usable ASIC gate count	214 K	407 K	941 K	1 M	1.7 M
Available SRAM	262 KBit	786 KBit	1 MBit	3.7 M	2.2 M
Number of metal layers	up to 7 (two layers are used for customer interconnect)				
Number of signal I/O pads	Up to 852				
System frequency	High-speed system frequency: up to 150 MHz system frequency and up to 250 MHz for local areas				
Gate power consumption	Combined circuit	0.0267 μW/MHz/gate			
	Sequential circuit	0.0215 μW/MHz/gate			
Power supply voltage	1.5 V ± 0.15 V				
Operating ambient temperature	-40 to +85 °C				
Interface voltage levels	1.5 V/2.5 V/3.3 V				
Base technology	Standard cell drawn 0.13 μm gate CMOS (UX-4 / CB-12)				

Package Line-up

	Number of balls	Ball Pitch (mm)	Body Size (mm ²)	Body Thickness (mm)
TBGA	352	1.27	35 x 35	1.40
	420	1.27	35 x 35	1.40
	500	1.27	40 x 40	1.40
	576	1.27	40 x 40	1.40
	680	1.00	40 x 40	1.40
ABGA	500	1.27	40 x 40	1.90
	756	1.27	45 x 45	1.90
	888	1.00	45 x 45	1.80
FCBGA	1155	1.00	35 x 35	3.16
	1521	1.00	40 x 40	3.16

Features

Architecture

The ISSP1 family is based on a 0.13 μm standard cell process. The user logic is implemented with CMGs. The high-performance process and the new concept allows system frequencies up to 150 MHz and up to 250 MHz for local areas.

Clock Tree and Design for Testability (DFT)

ISSP offers a complete concept for clock wiring: up to 32 local and 2 global clocks are integrated on the base-array. The local clocks are provided to areas, the global clock to the whole base-array. The clock trees are already embedded and fully balanced and shielded. All D flipflops are SCAN ready for implementing DFT with a minimum of effort. DFT methodologies such as SCAN, BSCAN and BIST are available and enable close to 100% testability.

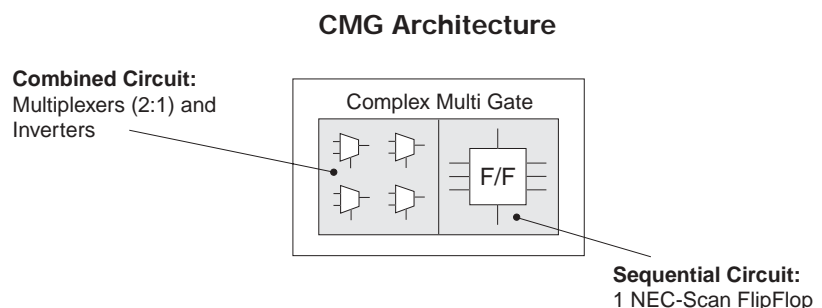
Deep Sub-Micron (DSM) Process

Normally for such an advanced process deep sub-micron effects have to be taken care of at layout time. With the complex multi-gate structure already predefined, DSM effects are already considered and no longer have an impact on the design. This allows for a short and reliable layout cycle.

Embedded Technology

CMGs

ISSP introduces the CMG, a new concept in the ASIC environment: CMGs consist of multiplexers, inverters and a register. The combinational and sequential circuits can be bypassed and used individually. This ensures that on-chip resources and performance can be maximized. The CMG concept also ensures a design flow free of DSM effects.



PLLs

4 analog PLLs are preintegrated: three high-speed PLLs with output frequencies between 25 MHz and 800 MHz and one mid-speed PLL with output frequency between 12.5 MHz and 400 MHz. Up to 32 DLLs are also embedded. This allows implementation of DDR or QDR interfaces.

SRAMs

The SRAMs on each base-array are divided into synchronous, dual-port 16-Kbit blocks. The selectable word count ranges from 256 to 16K with a bit width from 64 bits down to 1 bit. These embedded memories support system speeds up to 300 MHz. For the $\mu\text{PD65704/6}$ and $\mu\text{PD65705/7}$ dual-port-4-Kbit blocks are embedded.

Further Publications

This product letter contains preliminary specifications and operational data for the ISSP ASIC family. Additional information is available in NEC's ISSP design manual, block library and other related documents.

Contact your local NEC Design Center for further information (locations and phone numbers see below).

For more information on NEC's ASICs or other NEC products visit our European website at www.ee.nec.de

Contact

European Headquarters:

NEC Electronics (Europe) GmbH
Arcadiastr. 10, 40472 Düsseldorf, Germany
Tel. +49 211 65030
Fax +49 211 6503-1327
www.ee.nec.de

Offices in Europe:

www.ee.nec.de/europe

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