NEC

MOS INTEGRATED CIRCUIT
μPC121Cxx

LOW-SATURATION SERIES REGULATOR (LDO)

DESCRIPTION

The μPC121Cxx product is a series regulator with low output noise and high-ripple elimination characteristics that uses the Bi-CMOS process. It comes in a 0.4 mm thick chip-size package (CSP), which makes it ideal for portable terminals, which require high performance and compact size.

The internal circuit consists of a reference power supply, error amplifier, trimming resistors for output voltage setting, an overcurrent control circuit using fold-back current limiting, etc. In addition to its lower power consumption characteristics using MOSFET, the μPC121Cxx incorporates a low-saturation regulator and standby function, thus maximizing battery life.

FEATURES

- Output voltage accuracy : ±2% max. @ I_{OUT} = 30 mA, T_J = 25°C
  ±3% max. @ I_{OUT} = 30 mA, T_J = -40 to +125°C
- Regulator output current : 150 mA max.
- Output noise : 34 μVr.m.s. typ. @ 10 to 100 kHz
- Ripple elimination rate : 55 dB typ. @ 1 kHz, 52 dB typ. @ 10 kHz (V_{DIF} = 0.2 V)
- I/O voltage difference : T.B.D.
- Overload control : fold-back current limiting
- Package : 5-pin CSP 0.4 mm thickness (when mounted)

APPLICATIONS

- Cellular phones (W-CDMA, GSM, etc.)
- Portable terminals (DSC, DVC, PDA, games, AV, communication devices, etc.)

As a low-saturation 3-pin regulator, can replace general-purpose regulators.

ORDERING INFORMATION

Part Number	Package
μPC121Cxx	5-pin CSP
Packaging	Embossed tape

The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.
Not all products and/or types are availabe in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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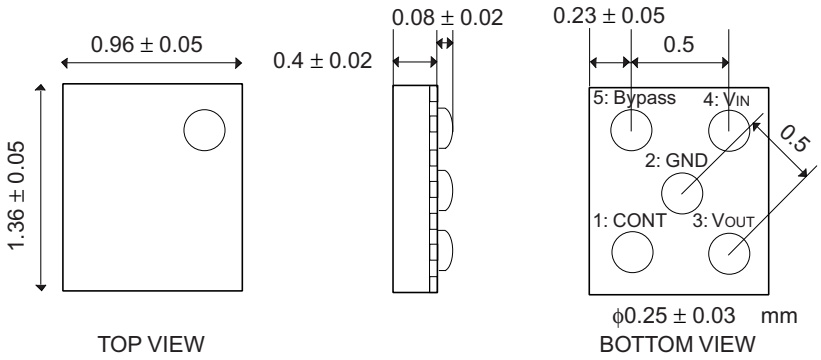
1. PACKAGE DRAWINGS (Unit: mm)

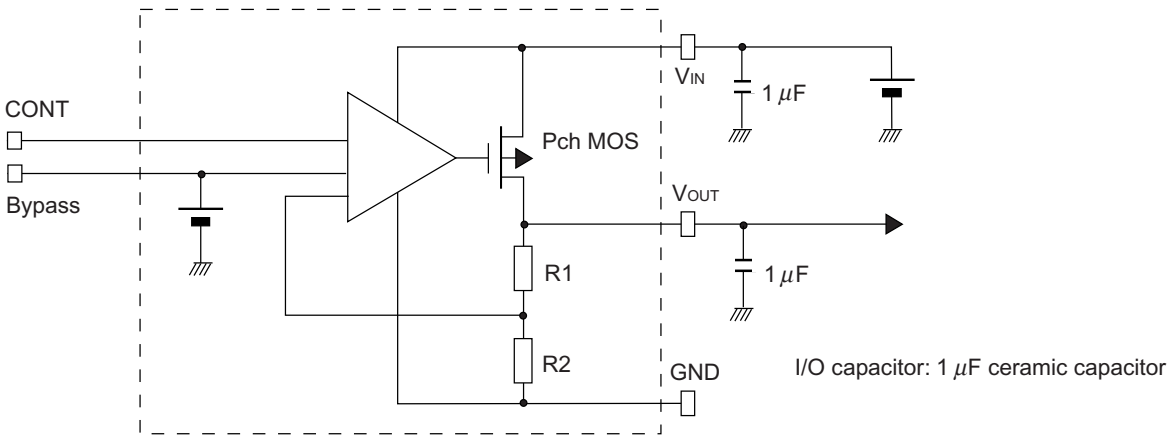


The top view surface is silicon that has been laser etched. The bottom view surface (mounting side) is epoxy resin coating, and the electrodes are formed of solder bumps.

2. PIN CONNECTIONS

Pin Number	Pin Name	Function
1	CONT	ON/OFF control pin (L = Standby mode, H = Active mode, pull-down resistor not connected)
2	GND	Ground pin
3	V_{OUT}	Output pin
4	V_{IN}	Input pin
5	Bypass	Noise reduction capacitor (0.01 μF) connection pin

3. INTERNAL CIRCUIT



- This IC compares the internal reference voltage and resistance split voltage, and controls the Pch MOSFETs to stabilize the output voltage.
- This IC performs fold-back current limiting when the load short circuit occurs. Protection functions for shutdown and thermal shutdown are not included.
- The input capacitor is a 1μF ceramic capacitor. If the wiring until the input and output capacitors is too long, the internal operational amplifier may oscillate, so connect the capacitors near the IC's input pin. Also make the V_{OUT}-V_{IN} wiring as short as possible, in order to minimize the wiring impedance.
- The control pin is not internally pulled up. Applying an intermediate voltage may cause abnormal operation or even physically damage the IC.

4. PRODUCT LINEUP

Part Number	Output Voltage	Output Current	Package	Marking	Taping
μ PC121C01	2.80 V± 2%	150 mA	5-pin CSP	Described	Embossed
μ PC121C01	2.85 V± 2%			separately	
μ PC121C02	2.90 V± 2%				
μ PC121C03	2.95 V± 2%				
μ PC121C04	3.0 V± 2%				

5. TAPING

Embossed tape 8 mm width, 4 mm pitch (EIAJ compliant)

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Input voltage	V_{IN}		–0.3 to +6.0	V
Output voltage	V_{OUT}		GND–0.3 to V_{IN} +0.3	V
Output current	I_{OUT}		±0.5	A
Control voltage	V_{CONT}		GND–0.3 to V_{IN} +0.3	V
Power consumption	P_T		0.244	W
Peak junction temperature	$T_{J\ (MAX)}$		125	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –40 to +85°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Maximum output current	$I_{D\ (DC)}$		+0.15		–	A

Electrical Characteristics (T_J = –40 to +125°C) Characteristic values are simulation values.

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage	V_{OUT}	I_{OUT} = 30 mA, T_J = 25°C, $V_{IN} = V_{OUT(C)}$ Note +0.5 V	–2	$V_{OUT(C)}$ Note	+2	%/V
		I_{OUT} = 30 mA, $V_{IN} = V_{OUT(C)}$ Note +0.5 V	–3	$V_{OUT(C)}$ Note	+3	%/V
Input stability	I_S	$V_{IN} = V_{OUT(C)}$ Note +0.5 V	–0.1		+0.1	%/V
Load stability	V_S	I_{OUT} = 1 to 150 mA	–	0.004	T.B.D.	%/mA
I/O voltage difference	V_{DIF1}	I_{OUT} = 30 mA			T.B.D.	mV
	V_{DIF2}	I_{OUT} = 150 mA			T.B.D.	mV
Circuit current	I_{DD}	$V_{CONT} \geq$ 1.4 V (H), I_{OUT} = 0 mA		84	150	μA
		$V_{CONT} \leq$ 1.4 V (L)			1.8	μA
Ripple elimination rate	PSRR	I_{OUT} = 50 mA, f = 1 kHz, $V_{IN} = V_{OUT(C)}$ Note + 0.2 V, T_J = 25°C		55		dB
		I_{OUT} = 50 mA, f = 10 kHz, $V_{IN} = V_{OUT(C)}$ Note + 0.2 V, T_J = 25°C		52		dB
		I_{OUT} = 50 mA, f = 1 kHz, $V_{IN} = V_{OUT(C)}$ Note + 1 V, T_J = 25°C		64		dB
		I_{OUT} = 50 mA, f = 10 kHz, $V_{IN} = V_{OUT(C)}$ Note + 1 V, T_J = 25°C		55		dB
Control current	I_{LIMIT}	$V_{IN} = V_{OUT(C)}$ Note + 0.5 V, Fold-back current limiting start current		300	T.B.D.	mA
Short circuit current	I_{SHORT}	V_{OUT} = GND		50		mA
Output noise	en	BW = 10 to 100 kHz, C_{OUT} = 1 μF, T_J = 25°C, Cbypass = 0.01 μF		34		μVr.m.s.
Rise time	T_{ON}	Cbypass = 0.01 μF (time from the instant control voltage exceeds V_{IH} until 95% of output voltage is reached)		150		μs
Control pin voltage	V_{IL}				0.4	V
	V_{IH}			1.4		V
Control pin leak current	I_{IL}	CONT = 0.4 V, V_{IN} = 6 V		1		nA

Note $V_{OUT(C)}$ refers to the central value of the well-stabilized output voltage when V_{IN}-0.5 V is input.

Remarks 1. T.B.D. (To be determined.)

2. The ripple elimination rate, output noise, and rise time are designed guaranteed values and cannot be tested.

7. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering this product.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

For more details, refer to the following.

"Semiconductor Device Mount Manual" (http://www.necel.com/pkg/en/mount/index.html)

Recommended Soldering Conditions for Surface Mount Type

μPC121Cxx: 5-pin CSP

Soldering Condition	Soldering Condition	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher) , Count: 3 times or less, Exposure limit: none, Flux: rosin based flux with less chlorine content (0.2 wt% or less) recommended	IR60-00-3

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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