

ASIC Technology

Product Letter

ISSP/150 nm
ISSP1 - High-Speed Interface Family

Description

The ISSP1-HSI, the Instant Silicon Solutions Platform™ (ISSP) High-Speed Interface (HSI) family, is a new class of ASIC device that features built-in, high-speed Serializer/Deserializer (SerDes) transceiver cores. Ideal for mid-volume designers of complex systems with high clock speeds and SerDes functionality, these devices are easily customizable using two metal layers to accommodate individual design requirements. Like ISSP1 standard devices, ISSP1-HSI devices generally are very easy to design, consume much less power than a comparable FPGA, and have NRE costs up to an order of magnitude lower than cell-based designs.

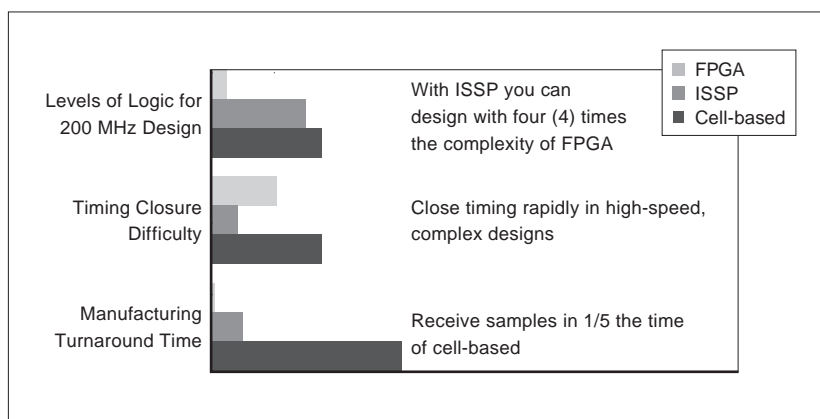
Design Performance, Turnaround Time Advantage

ISSP combines the best of both FPGA and cell-based technologies. It is based on NEC Electronics' production-proven 150 nm (UX4) CMOS process technology which provides the high performance required by many complex systems. At the same time, turnaround times are significantly reduced by using metal layers predefined for interconnection to embedded IP cores, design for test (DFT) circuits, clock domains, and power lines.

The time it takes to design a complex ASIC is becoming longer all the time, due to the need to insert and verify DFT circuitry and address deep submicron design issues such as signal integrity. Even in the FPGA world, it is not unusual to spend weeks to converge timing, especially for higher-utilized, large gate-count designs with clock speeds above 100 MHz.

Designers using ISSP need not worry about DFT problems causing delays to the design cycle because ISSP devices are preconfigured with testing methodologies such as SCAN, BSCAN, and others. Built-in clock domains further reduce design time by regulating timing intervals and lowering clock skew, while the high-performance process technology enables the clocks to operate at high speeds.

ISSP Design Performance



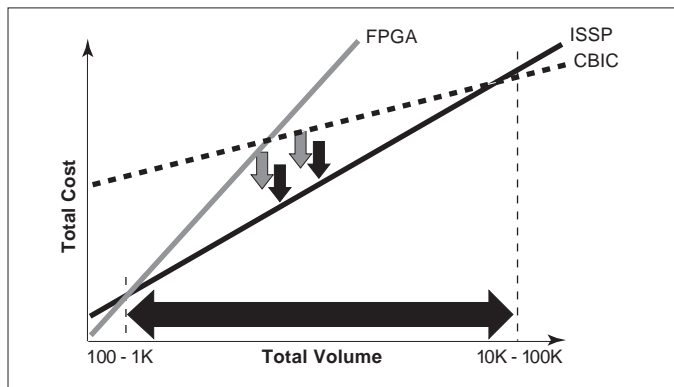
Turnaround Time Advantage

Benefits

Low-Risk Advantage

The rising costs for development and mask engineering of deep submicron ASICs make it difficult for designers of mid-volume products to target multiple respins of their prototypes. In the early stages of product design, it can be risky to try to predict the production volumes needed to amortize these development costs.

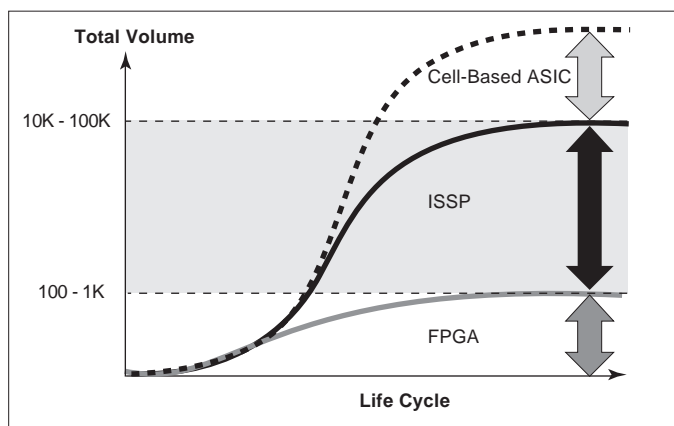
Total Volume vs. Total Cost



$$\text{Total Cost} = \text{Engineering Cost} + \text{Mask NRE} + \text{Total Volume} \times \text{Unit Cost}$$

By providing a high-performance solution, an easy design flow and NRE costs typically akin to those of a gate array, an ISSP allows fast respins of prototypes and enables products to reach mid-volume production levels at very reasonable costs. If the volumes need to increase, an ISSP designer can migrate easily to an NEC Electronics cell-based product that is built with the same process technology and based on the same IP and design flow.

Most Cost-Effective Device Zone



Product Features

Features

- Embedded SerDes transceiver cores (eight channels each)
 - 8- and 10-bit parallel interfaces
 - Supported data rates: 622 Mbps and 1.062, 1.25 and 2.5 Gbps
 - Physical layer (standard) compliance
 - PCI Express™
 - Gigabit Ethernet
 - Fibre Channel
- Embedded high-density SRAM
- Embedded FIFO SRAM
- Analog phase-locked loops (APLLs)
- Delay-locked loops (DLLs)
- Production-proven UX4 CMOS process technology; advanced 0.13µm (drawn) transistors
- System clock speeds up to 166 MHz
- 1.5 V core voltage
- Low power dissipation
- Complex multi-gate architecture in the user-defined logic area

Metal Layers

- Five to seven aluminum layers, depending on size of master and packaging type
- Lower three metal layers predefined for interconnection to
 - Embedded IP cores
 - Built-in testing (DFT) circuits
 - Clock domains
 - Power lines
- Next two metal layers allocated for customization of the target design
- One additional common layer to reinforce the power lines (in the largest master)
- Another common metal layer on top when using an FCBGA package

Sample Applications

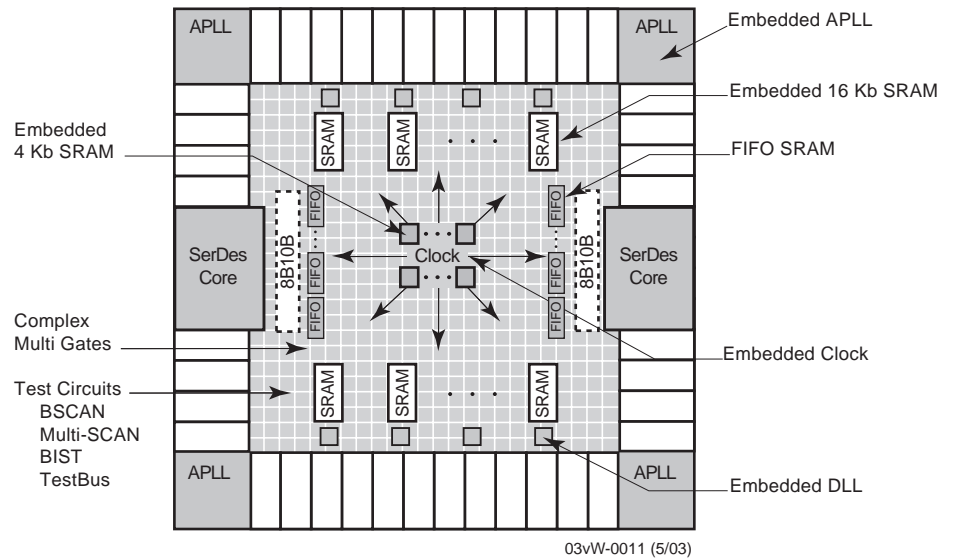
- High-performance broadband communication and networking equipment
- Mid-range and high-end server products and storage systems

Advantages

- Low overall development costs, engineering resources, mask NRE expenses
- Built-in DFT circuits, clocks, signal integrity and other features that simplify the design process and significantly reduce the customer's design effort
- Many other benefits associated with gate array, cell-based and even FPGA products
- Ability to leverage cell-based IP for fast and easy migration to cell-based designs
- Mid-volume production capabilities with very fast turnaround times
- Predictable flow for layout and turnaround times

Product Features (continued)

Chip Structure



Individual Specifications

Master	Usable Gates	Embedded SRAM			SerDes Channels	FIFO SRAM	Package
		16 Kb Blocks	4 Kb Blocks	Size (Bits)			
μPD65711	565K	42	0	729,088	8	32	576-, 756-ball ABGA
μPD65712	826K	56	0	917,504	16	64	576-, 756-, 888-ball ABGA
μPD65713	1.1M	112	20	1,916,928	16	64	756-, 888-ball ABGA
μPD65714	1.1M	112	20	1,916,928	16	64	1155-ball FCBGA

Note: Usable gates indicate equivalent ASIC gates, and include the NEC Electronics PCS firm core. Additional 130 K usable gates will be available if the PCS firm core is not used.

Product Features (continued)

Common Specifications (Preliminary)

Feature	Description
Process	0.15 μm (0.13 μm drawn) Si gate CMOS; six metal layers (seven for master $\mu\text{PD65714}$) ⁽¹⁾
Maximum usable gates	1.1M gates (usable) ⁽²⁾
Packages ⁽³⁾	576-, 756-, 888-ball ABGA; 1155-ball FCBGA
Supply voltage	Internal: 1.5V Interface: 2.5V / 3.3V and others for high-speed interface buffers
Power dissipation	Combinational circuit: 0.0267 $\mu\text{W}/\text{MHz}/\text{gate}$ Sequential circuit: 0.0215 $\mu\text{W}/\text{MHz}/\text{gate}$ (data line cycle/clock line cycle = 4)
Maximum local clock frequency	250 MHz
Maximum system clock frequency	166 MHz
Interfaces	3.3V LVTTTL; 2.5V LVCMOS 3.3V PCI, PCI-X (Mode1, Mode2) 3.3V LVDS, 2.5V LVDS, HSTL classes 1/3, SSTL18, SSTL2 classes 1/2, SSTL2 (differential) class 1, SSTL3 classes 1/2, LVPECL input
Embedded cores	Dual-port synchronous SRAM (~ 2.0 Mb max) – 16 Kb (1R/W+1R/W) compiled SRAM modules with 32-bit basis – 4 Kb (1R+1W) fixed SRAM modules; 64-bit x 64 word 8-channel SerDes transceiver cores (up to two depending on master) Fixed 10-bit x 128-word FIFO SRAM Four high-speed APLLs with eight-phase-shift function capability Slave DLLs for high-speed DRAM interface: – 8 for $\mu\text{PD65711}$ – 16 for $\mu\text{PD65712}$ – 32 for $\mu\text{PD65713}$ and $\mu\text{PD65714}$
Soft cores	Distributed compiled-type synchronous SRAM
Firm cores	8B/10B 10/100 Ethernet MAC, Gigabit Ethernet MAC DDR controller PCI controller UART Others
Embedded clocks	Two global clocks 32 local clocks
Embedded test circuits	SCAN, BSCAN, BIST, TestBus

Notes:

1. When using an FCBGA, one additional common layer is added on top.
2. The maximum available gate count is increased if the NEC Electronics PCS firm core is not used.
3. The number of usable signal pins depends on each package.

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