

## Specifications for the $\mu$ PD46128953

### Features

- 4,194,304 words by 32-bit organization
- Address inputs I/O data multiplex
- Operating ambient temperature:  $T_A = -25$  to  $+85$  °C
- Synchronous burst mode
  - Burst latency : 6/7/8
  - Burst sequence : Linear burst
  - Maximum clock frequency : 83 MHz
- SDR (Single Data Rate) Architecture
  - One data transfer per clock cycle
  - All inputs/outputs are synchronized with the positive edge of the clock
- Write data mask (DM) for write operation
- Output Enable: /OE pin
- Chip Enable input: /CE1 pin
- Standby Mode input: CE2 pin
- Standby Mode 1: Normal standby (128Mbit Memory cell data hold valid)
- Standby Mode 2: Density of memory cell data hold is variable (64M/32M/16M)
- Driver strength is variable (Strong/Middle/Weak)

### Operating voltage

Core: 1.7 to 2.0 V (1.85 $\pm$ 0.15 V)

I/O : 1.7 to 2.0 V (1.85 $\pm$ 0.15 V)

### Active current

30mA (Burst length 8)

### Operating ambient temperature

$T_A = -25$  to  $+85$  °C

### Package

127-pin plastic FBGA (13.0mm x 11.5mm)